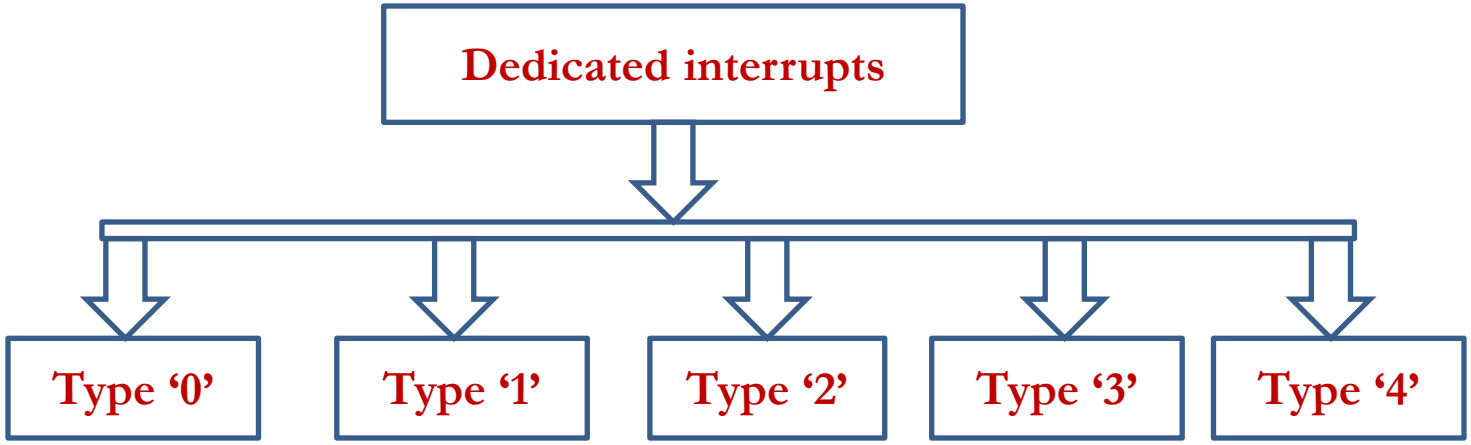
Dedicated interrupts

Learning Objectives

After going through this part of the lesson, you will be able to:

- Indentify the types of dedicated interrupts.
- Explain the uses of dedicated interrupts and their responses.

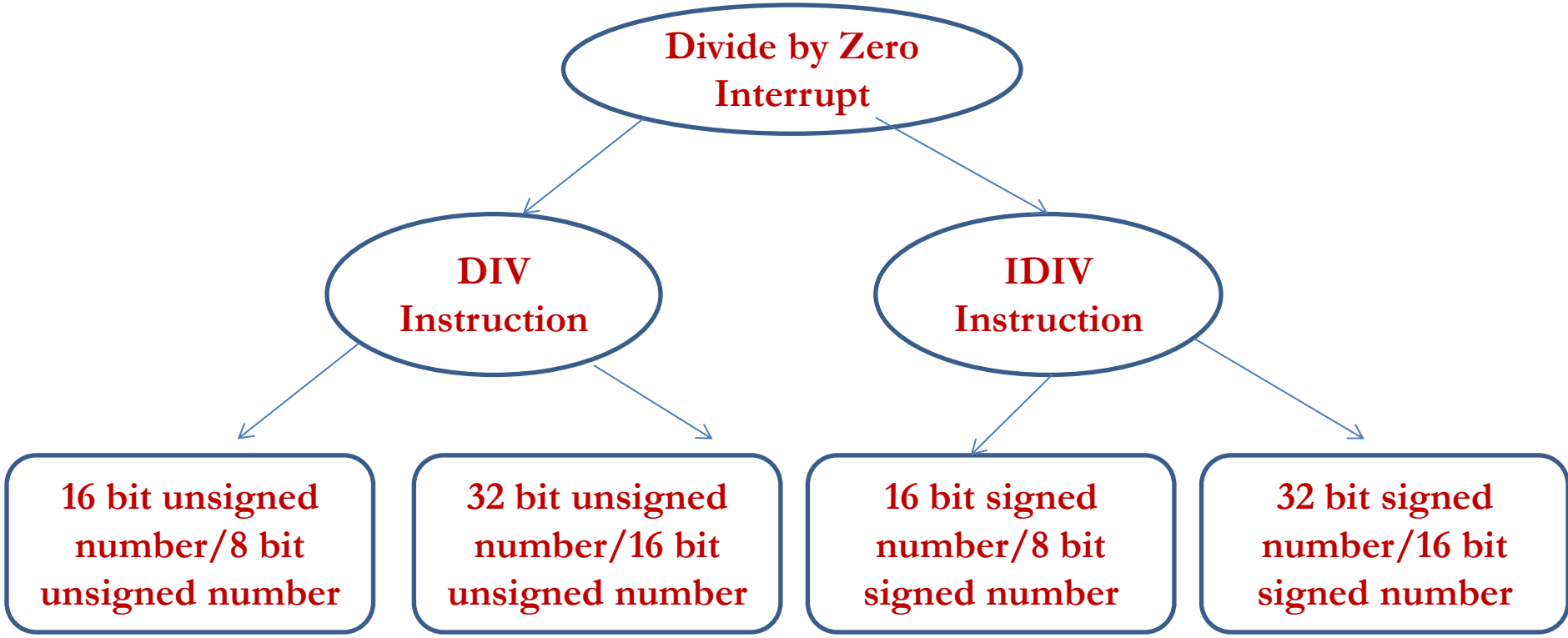
Types of Dedicated Interrupts



- **Type '0'** : Divide by Zero Interrupt
- **Type '1'** : Single Step Interrupt
- **Type '2'** : Non Maskable Interrupt
- **Type '3'** : Break Point Interrupt
- **Type '4'** :Overflow Interrupt

Type ‘0’ Interrupt

Type ‘0’ Interrupt / Divide by Zero Interrupt



Type '0' Interrupt (Cont..)

When this Divide by Zero Interrupt happens ?

Reasons :

1. Whenever the quotient from a DIV or IDIV is too large to fit in the result register, the 8086 processor will do an interrupt.
2. And whenever the divisor is Zero.

- After performing the 16 bit by 8 bit division, either signed or unsigned, the quotient part of the result is available in AL register, remainder is available in AH automatically.
- If the quotient result is more than 8 bits, which will not fit in AL register, then Divide by Zero interrupt occurs.

Type '0' Interrupt (Cont..)

Interrupt Response of Divide by Zero Interrupt

- After loading the starting address of the procedure which is written for Interrupt into CS & IP , then 8086 fetches and executes the first instruction of the ISR.

Type '0' Interrupt (Cont..)

It is written as INT 0 in the program.

- we can write the ISR routine which gives some message as "Divide by Zero Error Occurred"

- Example

  AX=0000 0010 0011 1010(570 decimal)

  BL=0000 0010(2 decimal)

  DIV BL ; AL=0001 1101 (29 decimal)

  ; Actual Quotient =1 0001 1101 (285), Remainder=0.

  ; incorrect because the result is too large to

  ; to fit in 8 bits (AL) then Divide by zero interrupt occurs

Type '1' Interrupt

Type '1' Interrupt / Single Step Interrupt

What is the use of this interrupt ?

- for debugging the programs.
- Type '1' ISR executes one instruction at a time and stop.
- Then we can examine the contents of registers and memory locations. If they are correct, next proceed to single step execution. Like wise we perform debugging the program using this interrupt.
- It is written as **INT 1** in the program.

Type '1' Interrupt (Cont..)

How to set/reset the trap flag ?

- There is no direct instruction to set the Trap Flag.
- The following program segment will set the Trap Flag

```
PUSHF                          ; Push flags on stack.
MOV BP,SP                      ; SP contents are copied into the
                               ; BP to act as indexed address
                               ;register.
OR WORD PTR[BP+0],0100H  ; Set Trap Flag (TF) bit
POPF                           ; The flag register contents are
                                        ; restored, along with TF=1.
```

- BP can not be used for indexed addressing with out displacement.

Type '1' Interrupt (Cont..)

- The following program segment will reset the Trap Flag

```
PUSHF                          ; Push flags on stack.
MOV BP,SP                      ; SP contents are copied into the
                               ; BP to act as indexed address
                               ;register.
AND WORD PTR[BP+0],0FEFFH  ; Reset Trap Flag (TF) bit
POPF                           ; The flag register contents are
                                        ; restored, along with TF=0.
```

Type '1' Interrupt (Contd..)

Interrupt Response of Single Step Interrupt

Type '2' Interrupt

Type '2' Interrupt / Nonmaskable Interrupt

- Why the term 'Nonmaskable' ?
- This interrupt can not be disabled by any program instructions.
- And can not be disabled intentionally or accidentally.
- 8086 executes the ISR written for Type '2' interrupt when it receives low-to-high transition on NMI input pin.
- It is written as INT 2 in program.

Type '2' Interrupt (Contd..)

Interrupt Response of Non maskable Interrupt

Type '2' Interrupt (Cont..)

Example: Pressure checking of steam from the boiler

What is response of the 8086 if pressure exceeds some limit ?

- Pressure sensor on a large steam boiler is connected to the NMI input of 8086 processor.
- If the pressure exceeds the some preset limit,

  the pressure sensor will send an interrupt signal to the 8086 through NMI.
- The ISR written for it might turn off the fuel to the boiler, open a pressure-relief valve, and sounds an alarm.

Type '3' Interrupt

Type '3' Interrupt / Break Point Interrupt

What is the use of this interrupt ?

- To implement a breakpoint function in a system.
- The breakpoint function also be used for debugging of the program.
- We can insert this INT 3 instruction in the program up to which we want to check (debug) it.
- The 8086 processor executes the instructions up to the INT 3 instruction. Then we can examine the contents of registers and memory locations by using appropriate commands.

Type '3' Interrupt (Contd..)

Interrupt Response of Break Point Interrupt

Type '4' Interrupt

Type '4' Interrupt / Overflow Interrupt

When this Overflow Interrupt happens ?

- If the result of the signed arithmetic operation is too large to be represented in the destination register or memory location, then Overflow flag will be set.
- Example

AL=01110011(+115 decimal)
BL=01001111(+79 decimal)
ADD AL,BL ; Sum is in AL
;AL=11000010 (- 62 decimal)
; incorrect because the result is too large to
; to fit in 7 bits, then OF=1

Type '4' Interrupt (Cont..)

- How to check the Overflow error ?
- There are two ways .

1. Write JO (Jump on Overflow) instruction, immediately after the Signed arithmetic instruction.

```
ADD AL,BL ;
JO address ; if OF=1, execution will jump to the
                    ; address specified
```

we can write the ISR routine which gives some message as "Overflow Error Occurred"

Type '4' Interrupt (Cont..)

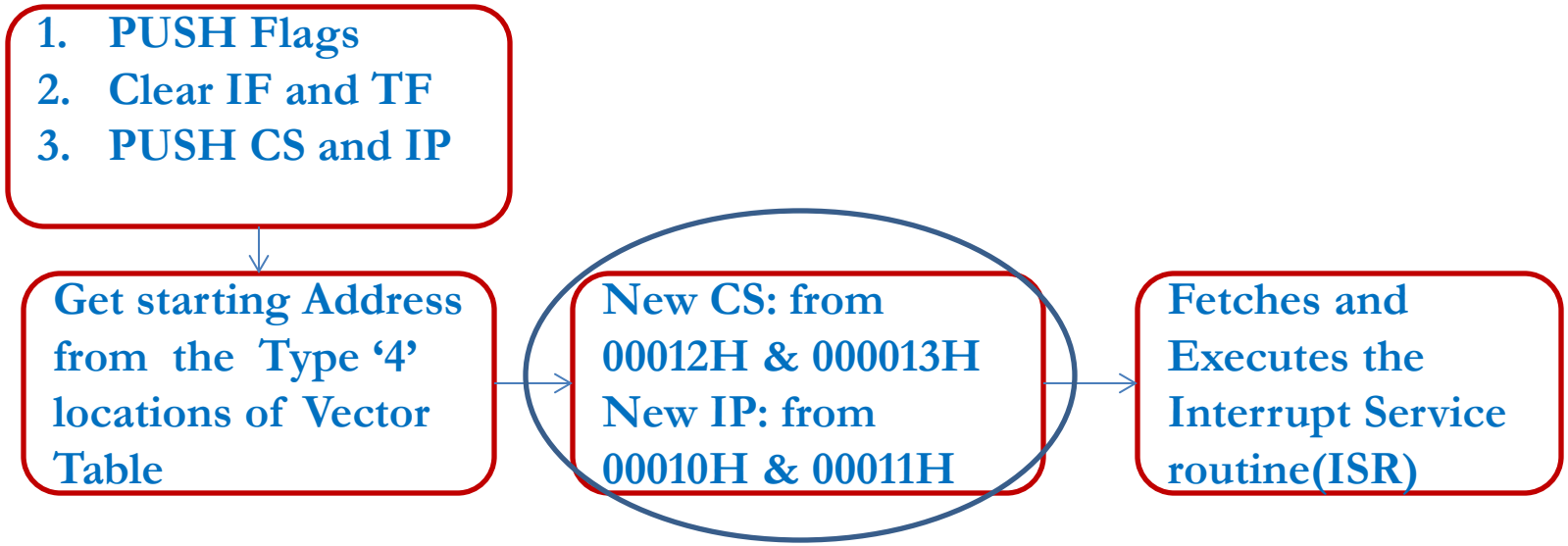
2. Write INTO(Interrupt on Overflow) instruction, immediately after the Signed arithmetic instruction.

```
ADD AL,BL ;
INTO          ; if OF=1, execution will jump to the
                ; address specified
```

we can write the ISR routine which gives some message as "Overflow Error Occurred"

Type ‘4’ Interrupt (Cont..)

Interrupt Response of Overflow Interrupt



Summary

- There are five dedicated interrupts.
- Each interrupt is used for specific purpose.
- Starting addresses of ISRs written for these are available in Interrupt vector table.
- In these NMI is hardware interrupt, remaining are software interrupts.

Source: Microprocessors and Interfacing, Douglas V Hall, TMH publications.

Thank You